iolinker Family Data Sheet

1 Introduction

1.1 Features

- IO extension with synchronized pin updates
- Dynamic IO matrix connections for signals up to 29.56 MHz
- UART / SPI / I2C interface, depending on chip version
- 7 hardware address pins that allow parallel connection of up to 127 uniquely addressable slaves
- Very few external components required, internal oscillator and PLL
- Instant on – powers up in microseconds
- Software reset and chip enable allow for quick and flexible set-ups, including multiplexing applications
- PWM generation
- Device operates with 1.2V or 1.8V / 2.5V / 3.3V

1.2 Introduction

The iolinker chip functions as a dynamically configurable IO matrix. Its main functionality, besides IO extension, is to dynamically set up a matrix of GPIO connections, that allow direct pass-through of high-frequency signals. Circuits can thereby be configured and programmed dynamically. There are UART / SPI / I2C versions that allow for easy integration of up to 127 chips connected in parallel. The chips also allow PWM signal output.

1.3 Applications

- I/O Port extender
- Large keypads
- Cable and wire control, short-circuit detection
- Software-based circuit configuration
- Simplified prototype boards, e.g. to wire up microcontrollers and periphery electronics on the fly
- User-configurable IO periphery interfaces
- Bus controller

- PWM controller, e.g. for huge LED panels
- Frequency generation

2 Interfaces

2.1 UART

The Universal Asynchronous serial Receiver and Transmitter (UART) is a serial communication device. The configuration used is as follows:

- Baud rate: 115200
- 8 data bits, 1 stop bit
- Parity: None
- LSB first

Note that this UART bus requires an external pull-up on its open collector TX line, as described in section 9.1.3.

A connection diagram can be seen in figure 1.

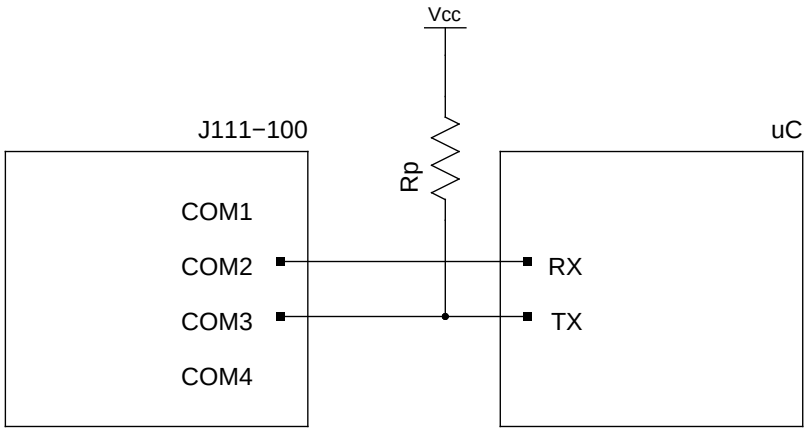

Figure 1: UART interface connection diagram

2.2 SPI

- Max. frequency: 4 MHz
- CPOL=0, CPHA=0 (SPI mode 0)
- MSB first

When the device is addressed, the master pulls the SS line low to initiate communication with the slave. The SS will be driven high to indicate the end of the current transaction.

A connection diagram can be seen in figure 2.

Signal	Description	Idle state
SCLK	Synchronous clock from the master to slaves	High
MOSI	Input line to the slaves from the master	High
MISO	Output line from the slaves to the master	Tristate
SS	Slave select	High

Table 1: SPI signal description

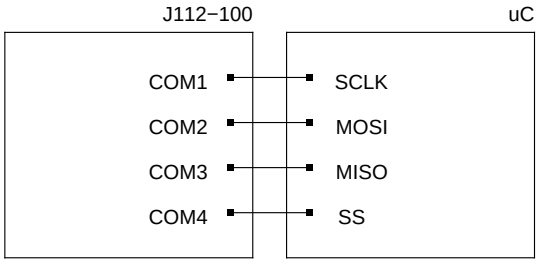

Figure 2: SPI interface connection diagram

2.3 I2C

Details to be announced.

A connection diagram can be seen in figure 3.

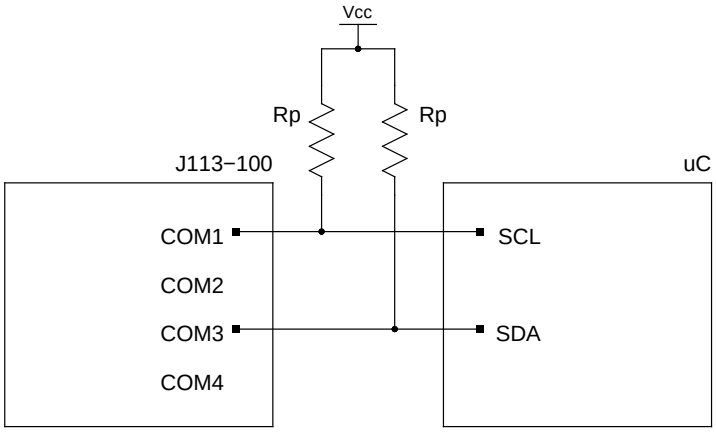

Figure 3: I2C interface connection diagram

2.4 Different Voltage Levels

Care has to be taken when connecting devices of different voltage levels.

To connect the iolinker 1.2V chips with devices of 3.3 V or less, the VCC_IO voltage level can be chosen appropriately. In other set-ups, level shifting is required.

3 Timing

3.1 SPI Protocol

When writing out an SPI command that requires a reply from the FPGA, the master has to keep writing out $n + 1$ zero bytes, where n is the number of bytes to be read back. This means that with one byte delay, the FPGA will begin sending out its response bytes.

3.2 Interrupt Pin

The interrupt pin INT notifies about state change of any GPIO currently configured as input. In idle mode it is open collector, which allows parallel connection of several chips on one shared interrupt line. An external pullup can keep it high.

When an interrupt occurs, the FPGA pulls the INT signal low for 10ms. After each low pulse a high pulse of at least 10ms length follows. Interrupts that occur during those 20ms are ignored.

4 Protocol

4.1 General Message Format

Messages **to** the device are of the format

Slave address	Command byte	Argument bytes	

Messages **from** the device are of the format

Reply argument bytes	

Replies are only sent for read operations (W=1, compare table 2).

The MSB of the command byte is always 1, and the MSB of all other bytes is 0. This makes it easy to recognize the start of a new message.

This general message format is slightly varied in SPI and in I2C mode, as described in the following sections.

4.2 SPI Message Format

Messages to the device	Command byte	Argument bytes	0x00	0x00	...	0x00
Messages from the device	–	–	–	Reply byte 1	...	Reply byte n

The slave address byte is left out, for slaves are selected via the Slave Select (SS) pin.

To read in the reply from the FPGA, the SPI master keeps sending out zero bytes $n + 1$ times after its command and command arguments. With one byte delay, the FPGA slave will write back its reply argument bytes.

4.3 I2C Message Format

Messages **to** the device are of the format

Command byte	Argument bytes

Messages **from** the device are of the format

Argument bytes

The slave address byte is left out, as it is encoded in the I2C protocol already.

4.4 Command Destination Address

The target address byte of the format 0sss ssss allows to target specific slave devices with a command. Each device processes messages only when addressed correctly with its user-defined slave address. The slave address can be configured through the hardware address pins as described in section 9.1.2.

The target address 0x7f holds a special function in the protocol, for it is always executed, regardless of the actual slave address. This allows to target all chips on the bus simultaneously.

Warning: Avoid using the universal slave address for read commands entirely when connecting multiple slaves. If multiple slaves were to reply to a read command simultaneously, they would cause a bus conflict and possible short circuit.

4.5 Command Encoding

The command byte is of the format 1W00 cccc.

W	Indicates if the operation is a Read (1) or a Write (0)
cccc	4 bit command number

Table 2: Command byte parameter description

The first nibble of the command byte therefore has the following possible values:

Hex	Binary	Function
0x8	0b1000	Write command
0xC	0b1100	Read command

Table 3: Command byte, first nibble

4.6 Command Buffer

Commands that change output pin states can be buffered. Buffered commands are not executed until a TRG message is received. Command buffering begins by issuing a SYN command.

4.7 Command List

4.7.1 VER – Retrieve chip version

Function	Return version and slave address
Command byte	0xC1
Argument list	–
Reply argument list	Version nibble, GPIO count nibble, LNK count nibble, PWM count nibble
Example reply arguments	0x16 0x63 (Version 1, 49 GPIOs, 49 LNK, 10 PWM)

The version nibble can hold any of the values in table 4.

Nibble	Description
0x0	Legacy version code (remaining nibbles do not conform to the described format)
0x1	iolinker original version
0x2	iolinker industry version

Table 4: Version nibble

The VER reply code 0x01 0x31 is a legacy version code of the original iolinker software version with 49 GPIOs, 49 LNK, 10 PWM.

The pin count encoding is done in accordance to table 5.

Nibble	Pin count
0x0	0
0x1	5
0x2	8
0x3	10
0x4	14
0x5	48
0x6	49
0x7	60
0x8	64
0x9	192

Table 5: Number encoding

4.7.2 TYP – Pin type set-up

Function	Sets pin type for the pin range x to y and remove all links that are in place
Command byte	0x82
Argument list	First pin address to change, last pin address to change, pin type
Example arguments	0x01 0x00 | 0x7f 0x00 | 0x03 (Define pins *P1* to *P127* as outputs)

If the last pin number equals 0, only one pin state will be changed.
The pin type can be any of the ones listed in table 6.

Pin type	Function
0x00	Low impedance / tristate
0x03	Output (Low initially)

Table 6: Pin type byte values

4.7.3 REA – Read register

Function	Read register address
Command byte	0xC7
Argument list	0x27 <addr> 0x00 0x00
Reply argument list	Register value
Example arguments	0x27 **0x7f** 0x00 0x00 (Read status register)

To read a register, use 0x27 as first argument byte, the register address according to table 7 as second byte, followed by 0x00 0x00.

Address	Function
0x7f	Status register

Table 7: Register addresses

The 7-bit register value will be returned in a single byte.

4.7.4 REA – Read pin states

Function	Read the state of pin range x to y
Command byte	0xC7
Argument list	First pin address to read, last pin address to read
Reply argument list	Current pin states
Example arguments	0x01 0x00 | 0x7f 0x00 (Read pins *P1* to *P127*)

To read pin states, use the first and the last pin address as parameters.
If the last pin number equals 0, only one pin state will be read. For pins that are not set as input pin, the state will always be returned as low.
The current pin states will be returned in $\left\lceil \frac{pin\_count}{7} \right\rceil$ bytes, and, if the pin count is not a multiple of 7, filled up with 0 bits on the LSB side.

4.7.5 SET – Set output states

Function	Sets pin range to high (= 1) or low (= 0) state
Command byte	0x83
Argument list	First pin address to set, last pin address to set, binary state of the write out
Example arguments	0x01 0x00 | 0x00 0x00 | 0x40 (set output pin *P1* to high state)

If the last pin number equals 0, only one pin state will be changed. Pins that are not of output type are skipped.

The binary state of the outputs is encoded in 1 byte per 7 pins. If the number of pins being set is not a multiple of 7, unused bits in the last byte are filled up with zeros from the LSB side.

Note that PWM output is only active for output pins in high state, i.e. this command can also be used to turn PWM on and off.

4.7.6 SYN – Synchronize Buffered IO State

Function	Enable command buffering
Command byte	0x88
Argument list	–

Use this command before you start issuing write commands you want to buffer. To end the buffer process, issue a TRG command.

4.7.7 TRG – Trigger IO State Buffer Execution

Function	Execute all buffered IO states (i.e. copy buffer to current and write out pin states)
Command byte	0x89
Argument list	–

Use this command to write out the buffered IO states, i.e. change all IO states in the same instant.

The buffering is thereby turned off and all future write commands will be executed instantaneously, until you execute another SYN command.

4.7.8 LNK – Set-up IO matrix

Function	Link output pin range to input/virtual pin z
Command byte	0x84
Argument list	First pin to set, last pin to set, target pin address
Example arguments	0x01 0x00 | 0x00 0x00 | 0x02 0x00 (Link pin *P1* to pin *P2*)

If the last pin number equals 0, only one pin state will be changed. Pins that are not of output type are skipped. If the target pin address is a physical pin, and said physical pin is of output type 0x03, it will be set to tristate input type.

If the LNK command is used on a pin where PWM output is currently active, LNK takes priority until cleared by the CLR command.

4.7.9 PWM – Configure Pulse Width Modulation

Function	Set PWM ratio for pin range
Command byte	0x85
Argument list	First pin to change, last pin to change, PWM ratio (PWM_R)
Example arguments	0x01 0x00 | 0x02 0x00 | 0x3f (This would set the pins *P1* and *P2* to a 50% PWM ratio, i.e. if LEDs were to be connected, they'd be on half brightness)

The PWM on/off ratio will be PWM_R:127.

The PWM_R argument byte has the format 0rrr rrrr, i.e. there are 128 possible values between 0 and 127, as seen in table 8.

PWM_R byte value	PWM ratio	PWM ratio in %
0x00	0:127	0%
0x01	1:127	0.8%
...	...	...
0x3f	63:127	49.6%
0x40	64:127	50.4%
...	...	...
0x7f	127:127	100%

Table 8: PWM_R byte values and their meaning

Note that the output state needs to be high for PWM output to be active.
To turn PWM off, set the PWM ratio to 100%.

4.7.10 CLR – Clear special pin functions

Function	Reset LNK settings for pin range
Command byte	0x8a
Argument list	First pin to change, last pin to change
Example arguments	0x01 0x00 | 0x02 0x00 (Reset pin links for *P1* to *P2*)

The clear command will unset pin links of a pin range.
If the last pin number equals 0, only one pin state will be changed. Pins that have been assigned no pin link function remain unchanged.

4.7.11 RST – Reset volatile memory

Function	Reset device state
Command byte	0x8f
Argument list	–

The software reset command will return the device to its default power-on state and lose all current settings.

5 Pin Addresses

Pin addresses are encoded in two bytes of the format 0PPPPPPP 00000PPP, where the first byte encodes the less significant 7 bits of the pin number, and the second byte encodes the more significant bits of the pin number. On devices with less than 128 pins, the second byte is always 0x00.

The second byte for pin numbers below 128 is therefore 0x00. Examples for physical pin addresses are listed in table 9.

Pin address	Function
0x01 0x00	Physical GPIO P1
0x02 0x00	Physical GPIO P2
0x03 0x00	...

Table 9: Physical pin addresses

6 Default Pin States

Pin	Default state
P1	Output, pull down
P2	Input
P3	Output, pull down
P4	Output, linked to P2
P5	Output, low
P6 – P49	Output, pull down

Table 10: Default pin states

7 Application Notes

7.1 Basic schematic for TQFP-100

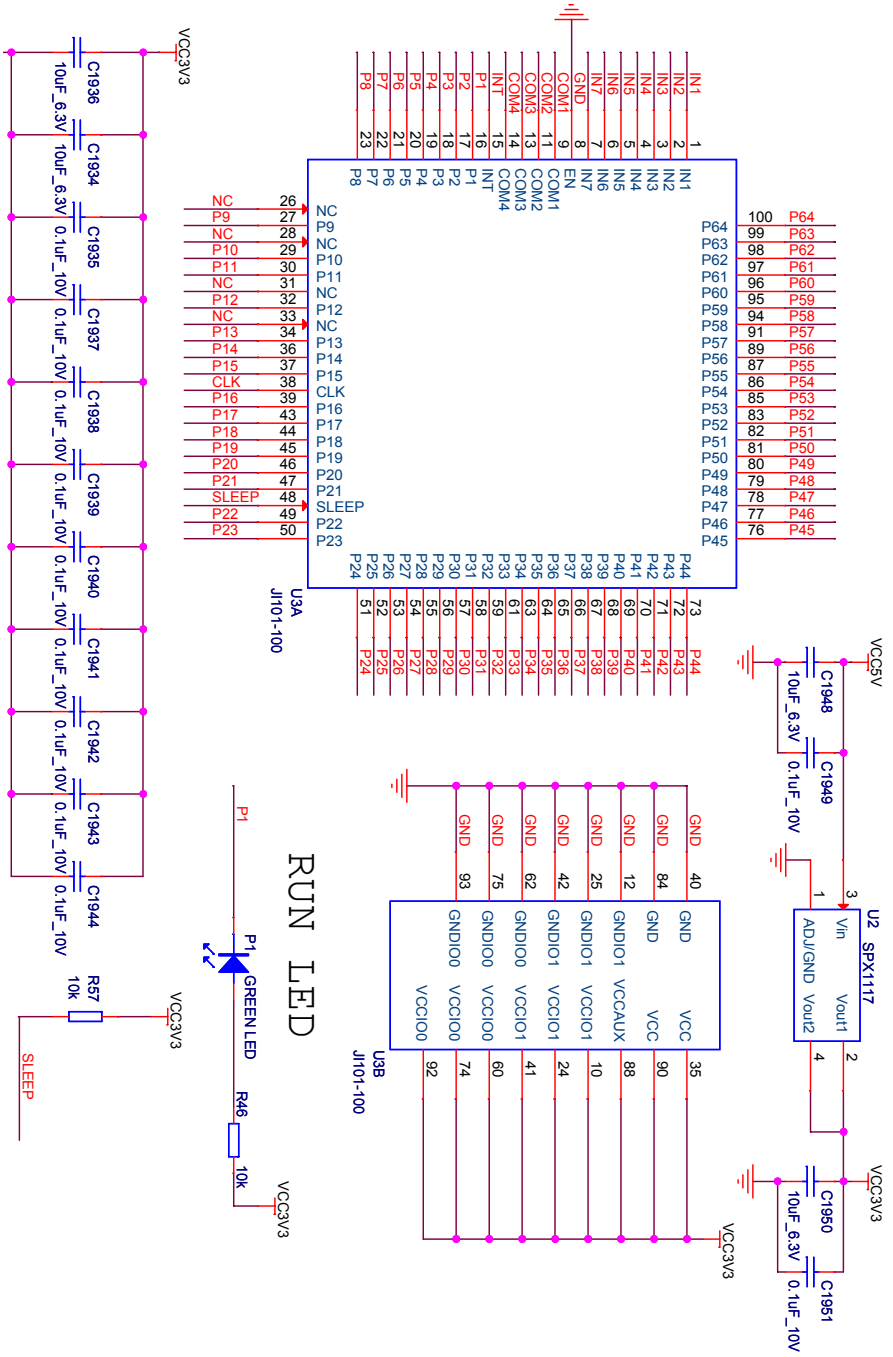

Figure 4: Basic schematic for TQFP-100 chips

7.2 Basic schematic for WLCSP-81

See JI11x-81L-B User Guide.

7.3 High Power LED Example

Using MOSFETs, the iolinker device can be used to control high power LEDs and entire LED panels.

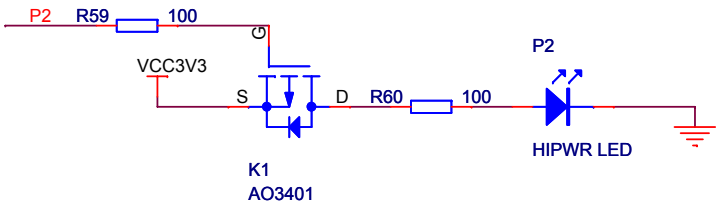

Figure 5: High power LED controller

8 Electrical Characteristics

8.1 Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage for 3.3V chips	1.71	3.465	V
V_{CCAUX}	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCIO}	I/O Driver Supply Voltage	1.14	3.465	V
t_{JCOM}	Junction Temperature	0	+85	°C

Table 11: Recommended Operating Conditions of 3.3V chips

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V/3.3 V Devices	2.375	3.465	V
V_{CCIO}	I/O Driver Supply Voltage	1.14	3.465	V
t_{JCOM}	Junction Temperature	0	85	°C

Table 12: Recommended Operating Conditions of 1.2V chips

8.2 Absolute Maximum Ratings

Parameter	3.3V chips
Supply Voltage V_{CC}	−0.5 to 3.75 V
Supply Voltage V_{CCAUX}	−0.5 to 3.75 V
Output Supply Voltage	−0.5 to 3.75 V
I/O Tristate Voltage Applied	−0.5 to 3.75 V
Dedicated Input Voltage Applied	−0.5 to 4.25 V
Storage Temperature (ambient)	−65 to 150 °C
Junction Temp. (T_j)	+125 °C

Table 13: Absolute Maximum Ratings of 3.3V chips

Parameter	1.2V chips Low Voltage	1.2V chips
Supply Voltage V_{CC}	−0.5 to 1.32 V	−0.5 to 3.75 V
Supply Voltage V_{CCAUX}	−0.5 to 3.75 V	−0.5 to 3.75 V
Output Supply Voltage	−0.5 to 3.75 V	−0.5 to 3.75 V
I/O Tristate Voltage Applied	−0.5 to 3.75 V	−0.5 to 3.75 V
Dedicated Input Voltage Applied	−0.5 to 3.75 V	−0.5 to 3.75 V
Storage Temperature (ambient)	−55 to 125 °C	−55 to 125 °C
Junction Temp. (T_j)	−40 to 125 °C	−40 to 125 °C

Table 14: Absolute Maximum Ratings of 1.2V chips

- Stress above the parameters listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.
- All voltages are referenced to GND.
- Overshoot and undershoot of −2 V to ($V_{IHMAX} + 2$) is permitted for a duration of < 20 ns.

8.3 Typical DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}	Input or I/O Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2\,V)$	—	—	10	µA
		$(V_{CCIO} - 0.2\,V) < V_{IN} \leq 3.6\,V$	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7V_{CCIO}$	−30	—	−150	µA
I_{PD}	I/O Active Pull-down Current	$V_{IL(MAX)} \leq V_{IN} \leq V_{IH(MAX)}$	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining current	$V_{IN} = V_{IL\,(MAX)}$	30	—	—	µA
I_{BHHS}	Bus Hold Low Overdrive current	$V_{IN} = 0.7V_{CCIO}$	−30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{IH\,(MAX)}$	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{IH\,(MAX)}$	—	—	−150	µA
V_{BHT}	Bus Hold Trip Points	$0 \leq V_{IN} \leq V_{IH\,(MAX)}$	$V_{IL(MAX)}$	—	$V_{IH(MIN)}$	V
C1	I/O Capacitance	$V_{CCIO} = 1.5\,V, \ldots, 3.3\,V$, V_{CC} = Typ., $V_{IO} = 0$ to $V_{IH(MAX)}$	—	8	—	pF
C2	Dedicated Input Capacitance	$V_{CCIO} = 1.5\,V, \ldots, 3.3\,V$, V_{CC} = Typ., $V_{IO} = 0$ to $V_{IH(MAX)}$	—	8	—	pF

Table 15: Typical DC Characteristics of 3.3V chips

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}	Input or I/O Leakage, Clamp ...	OFF, $V_{CCIO} < V_{IN} < V_{IH(MAX)}$	—	—	+175	µA
		OFF, $V_{IN} = V_{CCIO}$	−10	—	10	µA
		OFF, $V_{CCIO} - 0.97V < V_{IN} < V_{CCIO}$	−175	—	—	µA
		OFF, $0 < V_{IN} < V_{CCIO} - 0.97V$	—	—	10	µA
		OFF, V_{IN} = GND	—	—	10	µA
		ON, $V < V_{IN} < V_{CCIO}$	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	$0 < V_{IN} < 0.7V_{CCIO}$	−30	—	−309	µA
I_{PD}	I/O Active Pull-down Current	$V_{IL(MAX)} < V_{IN} < V_{CCIO}$	30	—	305	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL(MAX)}$	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7V_{CCIO}$	3 − 0	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	305	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	−309	µA
V_{BHT}	Bus Hold Trip Points		V_{IL} (MAX)	—	V_{IH} (MAX)	V
C1	I/O Capacitance	$V_{CCIO} = 1.2\,V, \ldots, 3.3\,V$ V_{CC} = Typ., $V_{IO} = 0$ to $V_{IH(MAX)}$	3	5	9	pF
C2	Dedicated Input Capacitance	$V_{CCIO} = 1.2\,V, \ldots, 3.3\,V$ V_{CC} = Typ., $V_{IO} = 0$ to $V_{IH(MAX)}$	3	5.5	7	pF
V_{HYST}	Hysteresis for Schmitt Trigger Inputs	$V_{CCIO} = 3.3\,V$ Hysteresis = Large	—	450	—	mV
		$V_{CCIO} = 2.5\,V$ Hysteresis = Large	—	250	—	mV
		$V_{CCIO} = 1.8\,V$ Hysteresis = Large	—	125	—	mV
		$V_{CCIO} = 1.5\,V$ Hysteresis = Large	—	100	—	mV
		$V_{CCIO} = 3.3\,V$ Hysteresis = Small	—	250	—	mV
		$V_{CCIO} = 2.5\,V$ Hysteresis = Small	—	150	—	mV
		$V_{CCIO} = 1.8\,V$ Hysteresis = Small	—	60	—	mV
		$V_{CCIO} = 1.5\,V$ Hysteresis = Small	—	40	—	mV

Table 16: Typical DC Characteristics of 1.2V chips

8.4 Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS3.3 (3.3 V chips)	−0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	4	−4
							8	−8
							12	−12
							16	−16
					0.2	$V_{CCIO} - 0.2$	0.1	−0.1
LVCMOS1.2 (1.2 V chips)	−0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	4	−2
							8	−6
					0.2	$V_{CCIO} - 0.2$	0.1	−0.1

Table 17: DC Electrical Characteristics of Single-Ended GPIOs

9 Pin Configurations

9.1 Signal Descriptions

9.1.1 General Pin Listing

Name	Pin type	Function	Note
EN	Input	Chip enable*	Pull low to activate chip
INT	Open collector output	Interrupt pin**	Use external pull-up

*When the chip is not enabled, all outputs are in their default state, pin links are inactive and no communication is processed.

**Informs about updates of input GPIOs, multiple devices can be connected on a single interrupt bus line.

Table 18: Enable and interrupt pin description

9.1.2 Slave Address Pin Listing

Name	Pin type	Function	Note
IN1	Input, internal pull-up	Slave address 1st bit, LSB	–
IN2	Input, internal pull-up	Slave address 2nd bit	–
IN3	Input, internal pull-up	Slave address 3rd bit	–
IN4	Input, internal pull-up	Slave address 4th bit	–
IN5	Input, internal pull-up	Slave address 5th bit	–
IN6	Input, internal pull-up	Slave address 6th bit	–
IN7	Input, internal pull-up	Slave address 7th bit, MSB	–

Table 19: Slave address pin description

The 7 bit slave address of the device can be assigned using the hardware address pins IN1 (LSB) to IN7 (MSB), which are connected to an internal pull-up resistor by default. The user can encode the slave address by puling the appropriate pins low. A high pin state is regarded as 1 bit, a low pin state as 0. Thus, if all pins are left unconnected, the slave address is 0x7f.

9.1.3 Communication Interface Pin Listing

Depending on chip version, the same hardware pins are used for one of the three communication interfaces, as described in table 20.

Note that the UART version requires an external pull-up (around 10kOhm) on its transmit pin, for it is designed to run on a shared open collector bus line. For the UART master, this approach is entirely transparent: Only the addressed iolinker chip will reply to any given message and pull low the UART transmit line. *To avoid harming any of the connected chips in case of incorrectly assigned slave addresses, that would lead to a bus conflict during replies, an additional 10kOhm resistor can be used to connect each individual device to the shared bus line.*

Name	Pin type	Function	Note
COM2	Input	UART Receive	Only available in iolinker UART version
COM3	Open collector output, external pull-up required	UART Transmit	
COM1	Input	SPI Clock	
COM2	Input	SPI MOSI	Only available in iolinker SPI version
COM3	Output	SPI MISO	
COM4	Input	SPI Slave Select	
COM1	Input	I2C Clock	Only available in iolinker I2C version
COM3	Open Collector Output	I2C Data	

Table 20: Communication pin description

9.2 WLCSP-36

Pin	Designation	Note	Pin	Designation	Note
A1	P1	GPIO / DONE	D1	**GND**	–
A2	P2	GPIO / PROGRAMN	D2	IN6	Slave address[5]
A3	**VCCIO0**	–	D3	P9	GPIO / TCK
A4	P3	GPIO	D4	IN7	Slave address[6] MSB
A5	P4	GPIO / TDI	D5	**VCC**	–
A6	IN1	Slave address[0] LSB	D6	EN	Chip enable, pull low to activate
B1	P5	GPIO / INITN	E1	COM4	NC[1], SPI SS[2], NC[3]
B2	CTRL	JTAGEN, use 10k pull-down to GND	E2	INT	Interrupt output
B3	CLK	Optional	E3	P10	GPIO
B4	P6	GPIO / TDO	E4	COM3	UART TX[1], SPI MISO[2], I2C Data[3]
B5	IN2	Slave address[1]	E5	P11	GPIO
B6	IN3	Slave address[2]	E6	P12	GPIO
C1	**VCC**	–	F1	COM2	UART RX[1], SPI MOSI[2], NC[3]
C2	P7	GPIO	F2	**VCCIO**	–

Table 21: Pin description WLCSP-36

Pin	Designation	Note	Pin	Designation	Note
C3	P8	GPIO / TMS	F3	P13	GPIO
C4	IN4	Slave address[3]	F4	P14	GPIO
C5	**GND**	–	F5	COM1	NC[1], SPI CLK[2], I2C SCL[3]
C6	IN5	Slave address[4]	F6	**VCCIO**	–

Table 21: Pin description WLCSP-36

[1]UART chip version
[2]SPI chip version
[3]I2C chip version

9.3 WLCSP-81

Pin	Designation	Note	Pin	Designation	Note
A1	**GND**	–	E6	P22	GPIO
A2	IN1	Slave address[0] LSB	E7	P23	GPIO
A3	IN2	Slave address[1]	E8	P24	GPIO
A4	**VCCIO**	–	E9	**VCC**	–
A5	IN3	Slave address[2]	F1	P25	GPIO
A6	IN4	Slave address[3]	F2	P26	GPIO
A7	P1	GPIO / TDI	F3	**VCC**	–
A8	P2	GPIO	F4	P27	GPIO
A9	**GND**	–	F5	P28	GPIO
B1	P3	GPIO / DONE	F6	P29	GPIO
B2	P4	GPIO	F7	P30	GPIO
B3	P5	GPIO	F8	P31	GPIO
B4	P6	GPIO	F9	**VCCIO**	–
B5	P7	GPIO	G1	COM4	NC[4], SPI SS[5], NC[6]
B6	CLK	Optional	G2	P32	GPIO
B7	P8	GPIO / TDO	G3	P33	GPIO
B8	IN5	Slave address[4]	G4	P34	GPIO
B9	IN6	Slave address[5]	G5	**GND**	–
C1	P9	GPIO / INITN	G6	**VCCIO**	–
C2	P10	GPIO / PROGRAMN	G7	P35	GPIO
C3	IN7	Slave address[6] MSB	G8	P36	GPIO
C4	**VCC**	–	G9	P37	GPIO
C5	**VCCIO**	–	H1	COM2	UART RX[4], SPI MOSI[5], NC[6]
C6	EN	Chip enable, pull low to activate	H2	P38	GPIO
C7	**VCCIO**	–	H3	P39	GPIO
C8	INT	Interrupt output	H4	P40	GPIO
C9	**VCCIO**	–	H5	P41	GPIO
D1	**VCC**	–	H6	P42	GPIO

Table 22: Pin description WLCSP-81

Pin	Designation	Note	Pin	Designation	Note
D2	CTRL	JTAGEN, use 10k pull-down to GND	H7	COM1	NC[4], SPI CLK[5], I2C SCL[6]
D3	P11	GPIO	H8	P43	GPIO
D4	P12 / TMS	GPIO	H9	P44	GPIO
D5	P13	GPIO	J1	**GND**	–
D6	P14	GPIO	J2	P45	GPIO
D7	P15	GPIO	J3	P46	GPIO
D8	P16	GPIO	J4	**VCCIO**	–
D9	P17	GPIO	J5	P47	GPIO
E1	P18	GPIO	J6	P48	GPIO
E2	P19	GPIO	J7	COM3	UART TX[4], SPI MISO[5], I2C Data[6]
E3	P20	GPIO	J8	P49	GPIO
E4	P21	GPIO / TCK	J9	**GND**	–
E5	**GND**	–			

Table 22: Pin description WLCSP-81

[4]UART chip version
[5]SPI chip version
[6]I2C chip version

9.4 TQFP-100

Pin	Designation	Note	Pin	Designation	Note
1	IN1	Slave address[0] LSB	51	P24	GPIO
2	IN2	Slave address[1]	52	P25	GPIO
3	IN3	Slave address[2]	53	P26	GPIO
4	IN4	Slave address[3]	54	P27	GPIO
5	IN5	Slave address[4]	55	P28	GPIO
6	IN6	Slave address[5]	56	P29	GPIO
7	IN7	Slave address[6] MSB	57	P30	GPIO
8	EN	Chip enable, pull low to activate	58	P31	GPIO
9	COM1	NC[7], SPI CLK[8], I2C SCL[9]	59	P32	GPIO
10	**VCC**	–	60	**VCCIO0**	–
11	COM2	UART RX[7], SPI MOSI[8], NC[9]	61	P33	GPIO
12	**GND**	–	62	**GNDIO0**	–
13	COM3	UART TX[7], SPI MISO[8], I2C Data[9]	63	P34	GPIO
14	COM4	NC[7], SPI SS[8], NC[9]	64	P35	GPIO
15	INT	Interrupt output	65	P36	GPIO
16	P1	GPIO	66	P37	GPIO
17	P2	GPIO	67	P38	GPIO
18	P3	GPIO	68	P39	GPIO
19	P4	GPIO	69	P40	GPIO
20	P5	GPIO	70	P41	GPIO
21	P6	GPIO	71	P42	GPIO
22	P7	GPIO	72	P43	GPIO
23	P8	GPIO	73	P44	GPIO
24	**VCCIO1**	–	74	**VCCIO0**	–
25	**GNDIO1**	–	75	**GNDIO0**	–
26	TMS	–	76	P45	GPIO

Table 23: Pin description TQFP-100

[7] UART chip version
[8] SPI chip version
[9] I2C chip version

Pin	Designation	Note	Pin	Designation	Note
27	P9	GPIO	77	P46	GPIO
28	TCK	–	78	P47	GPIO
29	P10	GPIO	79	P48	GPIO
30	P11	GPIO	80	P49	GPIO
31	TDO	–	81	P50	GPIO
32	P12	GPIO	82	P51	GPIO
33	TDI	–	83	P52	GPIO
34	P13	GPIO	84	**GND**	–
35	**VCC**	–	85	P53	GPIO
36	P14	GPIO	86	P54	GPIO
37	P15	GPIO	87	P55	GPIO
38	CLK	Optional	88	**VCCAUX**	–
39	P16	GPIO	89	P56	GPIO
40	**GND**	–	90	**VCC**	–
41	**VCCIO1**	–	91	P57	GPIO
42	**GNDIO1**	–	92	**VCCIO0**	–
43	P17	GPIO	93	**GNDIO0**	–
44	P18	GPIO	94	P58	GPIO
45	P19	GPIO	95	P59	GPIO
46	P20	GPIO	96	P60	GPIO
47	P21	GPIO	97	P61	GPIO
48	SLEEPN	Use 10k pull-up to VCC_3V3	98	P62	GPIO
49	P22	GPIO	99	P63	GPIO
50	P23	GPIO	100	P64	GPIO

Table 23: Pin description TQFP-100

9.5 CABGA-256

Pin	Designation	Note	Pin	Designation	Note
A1	**VCC**	–	J1	P93	GPIO
A2	NC	–	J2	P94	GPIO
A3	IN1	Slave address[0] LSB	J3	P95	GPIO
A4	IN2	Slave address[1]	J4	P96	GPIO
A5	IN3	Slave address[2]	J5	P97	GPIO
A6	P1	GPIO / TDI	J6	P98	GPIO
A7	P2	GPIO / TCK	J7	**VCCIO**	–
A8	CLK	Optional	J8	**GND**	–
A9	P3	GPIO	J9	**GND**	–
A10	IN4	Slave address[3]	J10	**VCCIO**	–
A11	IN5	Slave address[4]	J11	P99	GPIO
A12	IN6	Slave address[5]	J12	P100	GPIO
A13	P4	GPIO / INITN	J13	P101	GPIO
A14	IN7	Slave address[6] MSB	J14	P102	GPIO
A15	EN	Chip enable, pull low to activate	J15	P103	GPIO
A16	**VCC**	–	J16	P104	GPIO
B1	INT	Interrupt output	K1	P105	GPIO
B2	**GND**	–	K2	P106	GPIO
B3	P5	GPIO	K3	P107	GPIO
B4	P6	GPIO	K4	P108	GPIO
B5	P7	GPIO	K5	P109	GPIO
B6	P8	GPIO	K6	P110	GPIO
B7	P9	GPIO	K7	**VCC**	–
B8	P10	GPIO / TMS	K8	**VCCIO**	–
B9	P11	GPIO	K9	**VCCIO**	–
B10	P12	GPIO / PROGRAMN	K10	**VCC**	–
B11	P13	GPIO	K11	P111	GPIO
B12	P14	GPIO	K12	P112	GPIO
B13	P15	GPIO	K13	P113	GPIO
B14	P16	GPIO	K14	P114	GPIO
B15	**GND**	–	K15	P115	GPIO
B16	P17	GPIO	K16	P116	GPIO
C1	P18	GPIO	L1	P117	GPIO
C2	P19	GPIO	L2	P118	GPIO
C3	**GND**	–	L3	P119	GPIO
C4	P20	GPIO	L4	P120	GPIO
C5	P21	GPIO	L5	P121	GPIO

Table 24: Pin description CABGA-256

Pin	Designation	Note	Pin	Designation	Note
C6	P22	GPIO / TDO	L6	**GND**	–
C7	P23	GPIO	L7	P122	GPIO
C8	P24	GPIO	L8	P123	GPIO
C9	P25	GPIO	L9	P124	GPIO
C10	CTRL	JTAGEN, use 10k pull-down to GND	L10	P125	GPIO
C11	P26	GPIO	L11	**GND**	–
C12	P27	GPIO	L12	P126	GPIO
C13	P28	GPIO / DONE	L13	P127	GPIO
C14	**GND**	–	L14	P128	GPIO
C15	P29	GPIO	L15	P129	GPIO
C16	P30	GPIO	L16	P130	GPIO
D1	P31	GPIO	M1	P131	GPIO
D2	P32	GPIO	M2	P132	GPIO
D3	P33	GPIO	M3	P133	GPIO
D4	**GND**	–	M4	**VCCIO**	–
D5	**VCCIO**	–	M5	**GND**	–
D6	P34	GPIO	M6	P134	GPIO
D7	P35	GPIO	M7	P135	GPIO
D8	P36	GPIO	M8	P136	GPIO
D9	P37	GPIO	M9	P137	GPIO
D10	P38	GPIO	M10	P138	GPIO
D11	P39	GPIO	M11	P139	GPIO
D12	**VCCIO**	–	M12	**GND**	–
D13	**GND**	–	M13	**VCCIO**	–
D14	P40	GPIO	M14	P140	GPIO
D15	P41	GPIO	M15	P141	GPIO
D16	P42	GPIO	M16	P142	GPIO
E1	P43	GPIO	N1	P143	GPIO
E2	P44	GPIO	N2	P144	GPIO
E3	P45	GPIO	N3	P145	GPIO
E4	**VCCIO**	–	N4	**GND**	–
E5	**GND**	–	N5	**VCCIO**	–
E6	P46	GPIO	N6	P146	GPIO
E7	P47	GPIO	N7	P147	GPIO
E8	P48	GPIO	N8	P148	GPIO
E9	P49	GPIO	N9	P149	GPIO
E10	P50	GPIO	N10	P150	GPIO
E11	P51	GPIO	N11	P151	GPIO
E12	**GND**	–	N12	**VCCIO**	–

Table 24: Pin description CABGA-256

Pin	Designation	Note	Pin	Designation	Note
E13	**VCCIO**	–	N13	**GND**	–
E14	P52	GPIO	N14	P152	GPIO
E15	P53	GPIO	N15	P153	GPIO
E16	P54	GPIO	N16	P154	GPIO
F1	P55	GPIO	P1	P155	GPIO
F2	P56	GPIO	P2	P156	GPIO
F3	P57	GPIO	P3	**GND**	–
F4	P58	GPIO	P4	P157	GPIO
F5	P59	GPIO	P5	P158	GPIO
F6	**GND**	–	P6	COM1	NC[10], SPI CLK[11], I2C SCL[12]
F7	P60	GPIO	P7	P159	GPIO
F8	P61	GPIO	P8	P160	GPIO
F9	P62	GPIO	P9	P161	GPIO
F10	P63	GPIO	P10	P162	GPIO
F11	**GND**	–	P11	P163	GPIO
F12	P64	GPIO	P12	P164	GPIO
F13	P65	GPIO	P13	COM2	UART RX[10], SPI MOSI[11], NC[12]
F14	P66	GPIO	P14	**GND**	–
F15	P67	GPIO	P15	P165	GPIO
F16	P68	GPIO	P16	P166	GPIO
G1	P69	GPIO	R1	P167	GPIO
G2	P70	GPIO	R2	**GND**	–
G3	P71	GPIO	R3	P168	GPIO
G4	P72	GPIO	R4	P169	GPIO
G5	P73	GPIO	R5	P170	GPIO
G6	P74	GPIO	R6	P171	GPIO
G7	**VCC**	–	R7	P172	GPIO
G8	**VCCIO**	–	R8	P173	GPIO
G9	**VCCIO**	–	R9	P174	GPIO
G10	**VCC**	–	R10	P175	GPIO
G11	P75	GPIO	R11	P176	GPIO

Table 24: Pin description CABGA-256

[10] UART chip version
[11] SPI chip version
[12] I2C chip version

Pin	Designation	Note	Pin	Designation	Note
G12	P76	GPIO	R12	COM4	NC[10], SPI SS[11], NC[12]
G13	P77	GPIO	R13	P177	GPIO
G14	P78	GPIO	R14	P178	GPIO
G15	P79	GPIO	R15	**GND**	–
G16	P80	GPIO	R16	P179	GPIO
H1	P81	GPIO	T1	**VCC**	–
H2	P82	GPIO	T2	P181	GPIO
H3	P83	GPIO	T3	P182	GPIO
H4	P84	GPIO	T4	P183	GPIO
H5	P85	GPIO	T5	P184	GPIO
H6	P86	GPIO	T6	COM3	UART TX[10], SPI MISO[11], I2C Data[12]
H7	**VCCIO**	–	T7	P185	GPIO
H8	**GND**	–	T8	P186	GPIO
H9	**GND**	–	T9	P187	GPIO
H10	**VCCIO**	–	T10	P180	GPIO
H11	P87	GPIO	T11	P188	GPIO
H12	P88	GPIO	T12	P189	GPIO
H13	P89	GPIO	T13	P190	GPIO
H14	P90	GPIO	T14	P191	GPIO
H15	P91	GPIO	T15	P192	GPIO
H16	P92	GPIO	T16	**VCC**	–

Table 24: Pin description CABGA-256

10 Ordering Information

Ordering Code	Package	Pin count	GPIO	LNK	PWM	Interface	VCC_core
JI107-100	TQFP-100	100	60	0	0	UART	1.8 V/2.5 V/3.3 V
JI108-100	TQFP-100	100	60	0	0	SPI	1.8 V/2.5 V/3.3 V
JI109-100	TQFP-100	100	60	0	0	I2C	1.8 V/2.5 V/3.3 V
JI111-36L	WLCSP-36	36	14	14	8	UART	1.2 V
JI112-36L	WLCSP-36	36	14	14	8	SPI	1.2 V
JI113-36L	WLCSP-36	36	14	14	8	I2C	1.2 V
JI114-36L	WLCSP-36	36	14	8	14	UART	1.2 V
JI115-36L	WLCSP-36	36	14	8	14	SPI	1.2 V
JI116-36L	WLCSP-36	36	14	8	14	I2C	1.2 V
JI111-81L	WLCSP-81	81	49	49	10	UART	1.2 V
JI112-81L	WLCSP-81	81	49	49	10	SPI	1.2 V
JI113-81L	WLCSP-81	81	49	49	10	I2C	1.2 V
JI114-81L	WLCSP-81	81	49	10	49	UART	1.2 V
JI115-81L	WLCSP-81	81	49	10	49	SPI	1.2 V
JI116-81L	WLCSP-81	81	49	10	49	I2C	1.2 V
JI117-256	CABGA-256	256	192	0	0	UART	2.5 V/3.3 V
JI118-256	CABGA-256	256	192	0	0	SPI	2.5 V/3.3 V
JI119-256	CABGA-256	256	192	0	0	I2C	2.5 V/3.3 V

Table 25: iolinker versions

VCCIO for all chips is 1.14 to 3.465V.

11 Packaging Information

Package	Spacing	Size
WLCSP-36	0.4 mm	2.5 × 2.5 mm
WLCSP-81	0.4 mm	3.8 × 3.8 mm
TQFP-100	0.5 mm	14 × 14 mm
CABGA-256	0.8 mm	14 × 14 mm

Table 26: Packaging information for chip models

12 Errata

The revision letter in this section refers to the revision of the iolinker device.

12.1 iolinker Rev. A

Initial release.

13 Revision History

Date	Version	Change Summary
September 2016	1	Initial release.
December 2016	2	Revised datasheet to match new products.
January 2017	3	Corrected pin listing for WLCSP-81.
January 2017	4	Corrected argument listing for TYP command.
March 2017	5	Minor corrections, timing and SPI elaborations.
April 2017	6	Added 'Default Pin States' section, corrected EN pin function footnote in 'Pin Configurations' section.
September 2017	7	Corrected pin listing for WLCSP-36 and CABGA-256.
November 2017	8	More extensive version numbering scheme for VER command.

Table 27: Data sheet revision history

Contents