User Guide
iolinker Evaluation Board JI11x-81L-B

1 Features

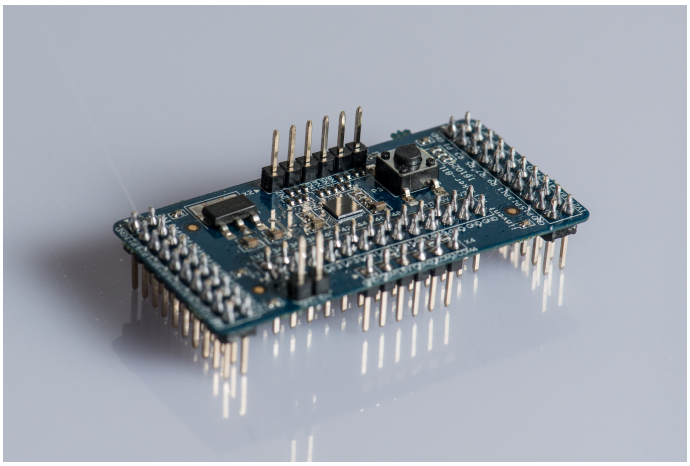

Figure 1: Product illustration

The evaluation board for the JI11x-81L chips is a Lattice MachXO3 FPGA board with 49 GPIOs.

FPGA	LCMXO3L-4300E-5UWG81CTR50
Supply voltage	3.3 V – 5 V, MicroUSB for power supply available
VCC_IO	3.3 V with internal voltage regulator, can be manually changed to 1.2 V – 3.465 V
VCC_core	1.2 V with internal voltage regulator
JTAG port	Yes, compatible with Lattice JTAG cables
GPIO list	P1 - P49 freely usable as GPIOs, INT is a freely usable GPIO meant for interrupt signals, COM1-4 are GPIOs meant for communication interface usage (e.g. UART, SPI or I2C), IN1-7 GPIOs for address encoding and hard-wired to GND, EN meant as reset pin

Table 1: Hardware feature list

For details on the preprogrammed software, please refer to the iolinker chip datasheet.

2 Pin Configurations

Pin	Designation	Function	Pin	Designation	Function
A1	**GND**	–	E6	P22	GPIO
A2	IN1	Slave address[0] LSB	E7	P23	GPIO
A3	IN2	Slave address[1]	E8	P24	GPIO
A4	**VCCIO**	–	E9	**VCC**	–
A5	IN3	Slave address[2]	F1	P25	GPIO
A6	IN4	Slave address[3]	F2	P26	GPIO
A7	P1	GPIO / TDI	F3	**VCC**	–
A8	P2	GPIO / Push button	F4	P27	GPIO
A9	**GND**	–	F5	P28	GPIO
B1	P3	GPIO / DONE	F6	P29	GPIO
B2	P4	GPIO / LED	F7	P30	GPIO
B3	P5	GPIO / LED	F8	P31	GPIO
B4	P6	GPIO	F9	**VCCIO**	–
B5	P7	GPIO	G1	COM4	NC[1], SPI SS[2], NC[3]
B6	CLK	Optional	G2	P32	GPIO
B7	P8	GPIO / TDO	G3	P33	GPIO
B8	IN5	Slave address[4]	G4	P34	GPIO
B9	IN6	Slave address[5]	G5	**GND**	–
C1	P9	GPIO / INITN	G6	**VCCIO**	–
C2	P10	GPIO / PROGRAMN	G7	P35	GPIO
C3	IN7	Slave address[6] MSB	G8	P36	GPIO
C4	**VCC**	–	G9	P37	GPIO
C5	**VCCIO**	–	H1	COM2	UART RX[1], SPI MOSI[2], NC[3]
C6	EN	Chip enable, pull low to activate	H2	P38	GPIO
C7	**VCCIO**	–	H3	P39	GPIO
C8	INT	Interrupt output	H4	P40	GPIO
C9	**VCCIO**	–	H5	P41	GPIO
D1	**VCC**	–	H6	P42	GPIO

Table 2: Pin description WLCSP-81

Pin	Designation	Function	Pin	Designation	Function
D2	JTAGEN	Use 10k pull-down to GND	H7	COM1	NC[1], SPI CLK[2], I2C SCL[3]
D3	P11	GPIO	H8	P43	GPIO
D4	P12 / TMS	GPIO	H9	P44	GPIO
D5	P13	GPIO	J1	**GND**	–
D6	P14	GPIO	J2	P45	GPIO
D7	P15	GPIO	J3	P46	GPIO
D8	P16	GPIO	J4	**VCCIO**	–
D9	P17	GPIO	J5	P47	GPIO
E1	P18	GPIO	J6	P48	GPIO
E2	P19	GPIO	J7	COM3	UART TX[1], SPI MISO[2], I2C Data[3]
E3	P20	GPIO	J8	P49	GPIO
E4	P21	GPIO / TCK	J9	**GND**	–
E5	**GND**	–			

Table 2: Pin description WLCSP-81

Take special care when using GPIOs that hold a second function as JTAG pins and compare with the schematic to verify that they are not pulled up externally.

[1]UART chip version
[2]SPI chip version
[3]I2C chip version

3 Special GPIOs

These pins are normal GPIOs, but in the iolinker application hold special meaning.

3.1 Enable

The EN pin is a pullup in the iolinker application. With a jumper it can be connected to GND on the board to activate the GPIOs P1 - P49. As P1 - P49 is open collector otherwise, this can also be used for multiplexing.

3.2 Interrupt

The INT pin is defined as an open collector pin with external pullup, that can be connected in parallel between multiple boards. The iolinker application notifies about input pin changes with a 10ms low signal on this pin.

3.3 Communication interface

Pin	UART	SPI	I2C
COM1	–	CLK	Clock
COM2	RX	MOSI	–
COM3	TX (open collector when idle)	MISO	Data
COM4	–	SS	–

Table 3: Communication pins

COM1 - COM3 can always be connected in parallel, when using multiple boards.

3.4 Address encoding

The 0K resistors marked as IN1 - IN7 on the front silkscreen connect to GND. When the FPGA software uses an internal pullup on those pins, the resistors can be used for encoding static configuration options, such as slave addresses.

In the iolinker application, IN1 is the least significant bit of the slave address, and IN7 the most significant bit. A GND connection encodes a 0 bit. The default slave addresses is therefore 0x00. By removing IN1, it could be changed to 0x01, etc.

4 Changing VCC_IO

If you intend to change VCC_IO to another voltage than the $3.3\,\mathrm{V}$ used by default, remove resistors R71 and R75. Then connect at least one pad (near the FPGA) to another voltage between $1.2\,\mathrm{V}$ and $3.465\,\mathrm{V}$. On the connector X7, pin 20 is unused and can be repurposed. *Take care to not damage the FPGA when soldering.*

After changing VCC_IO, the input and output voltage level of all GPIOs will change. This includes the JTAG interface. Please make sure that your JTAG cable supports the new voltage.

5 JTAG interface

5.1 Hardware preparation

To program the FPGA, connect the pins from your JTAG programming cable to the board as listed in table 4.

JTAG cable pin	Board pin	Header	
TDI	TDI	X2	
TDO	TDO	X2	
TMS	TMS	X2	
TCK	TCK	X2	
GND	GND	X2	
PROG	JTAGEN	X2	
VCC	VCC_IO	X5, X6 or X7	
INIT	–	–	
TRST	–	–	

Table 4: JTAG programmer connections

5.2 Usage of the programming software

In the Lattice Programmer utility, create a new blank project. In the right bar, choose "Custom I/O settings" and select "ispEN connect: high" as can be seen in figure 2. (This will pull JTAGEN high when programming and thereby enable the JTAG pins on the FPGA board.)

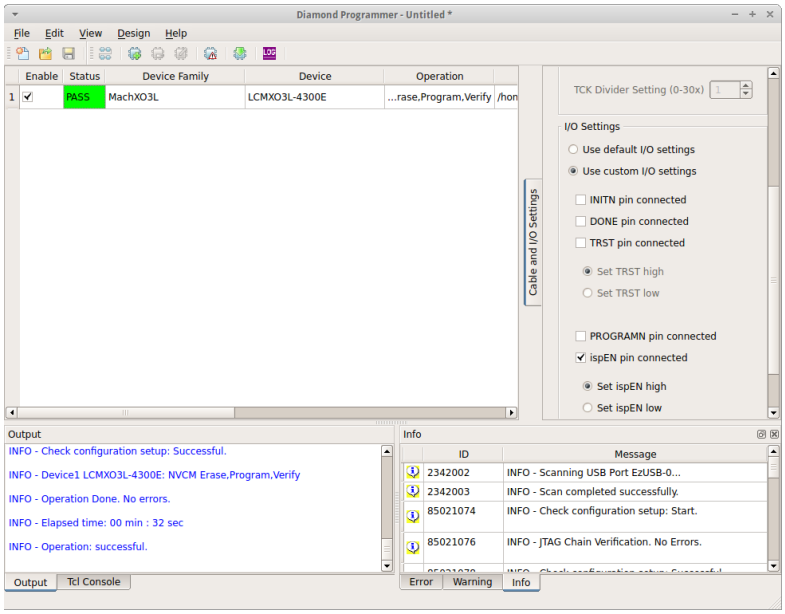

Figure 2: The Lattice Programmer software

Click the "JTAG Scan" button. The FPGA should be recognized and identified automatically. If it fails, don't forget to verify that the just made "Custom I/O settings" are still in effect before retrying.

Choose "Erase, Program, Verify" as operation and select a *.jed file. You can now click "Program" to transfer your new application onto the board.

Be careful: NVCM programming can only be done 9 times. For software testing, choose "Static RAM Cell Mode" instead. What you program into RAM is reset after the next power cycle, however.

5.3 Troubleshooting

Reasons for failure may be:

- Software issues – particularly verify that the programmer cable is recognized and the custom I/O settings have been made; other USB serial devices or cables may cause issues as well
- Issues with your JTAG cable
- Wrong wiring
- Board not supplied with power
- VCC_IO not in the allowed voltage range of your JTAG cable
- Damaged hardware

As a first step, always verify your wiring and the VCC_IO voltage.

6 Schematic

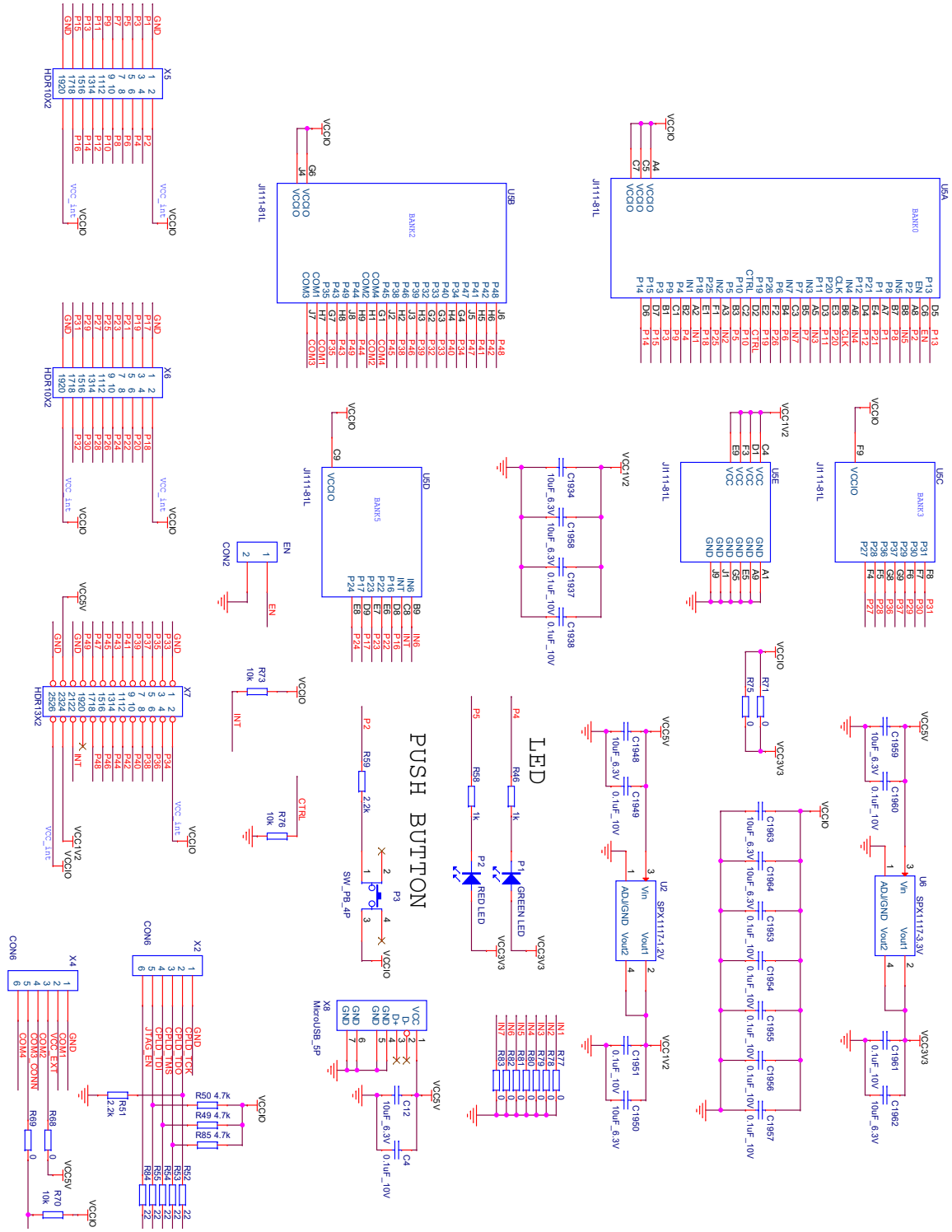

Figure 3: Schematic

7 Assembly Drawing

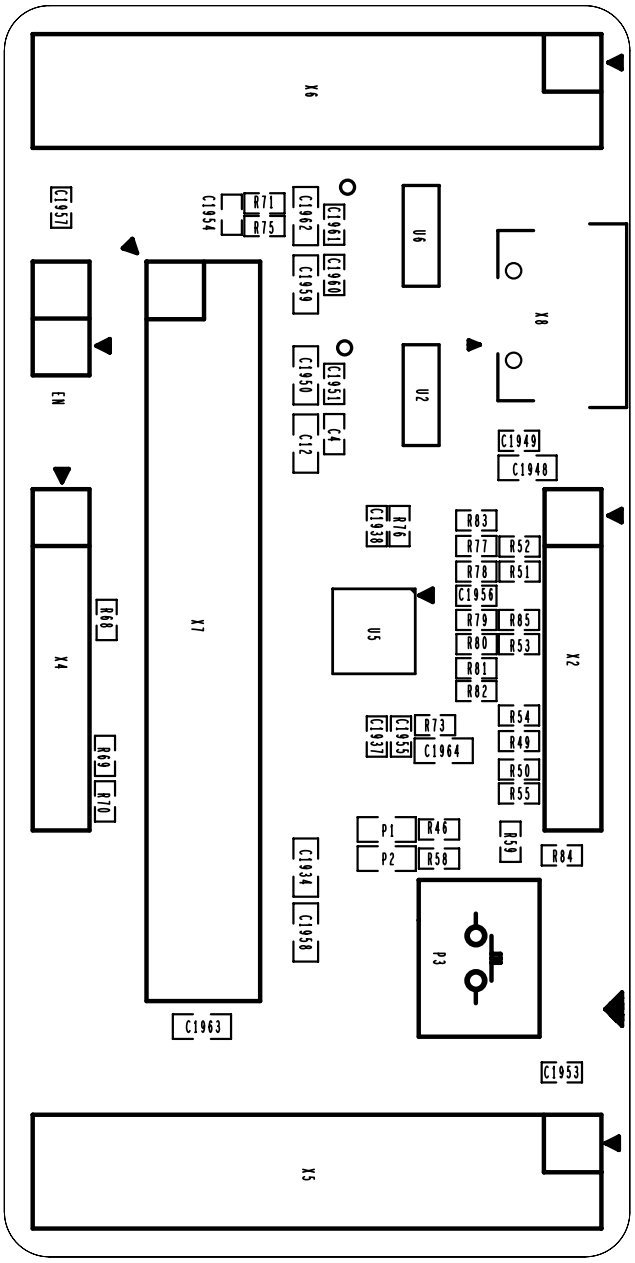

Figure 4: Assembly drawing

Contents